# 产 品 承 认 书
# SPECIFICATIONS

品 名（Module Name）： Q3S06A

客户型号（Cust.P/N）：

文档接受时间（Received）：

DATE: / /

| 客 户 名 称 (Customer) | | |
|---|---|---|
| 批 准 (Approved) | 审 核 (Checked) | 担 当 (In charge) |
| | | |

产品承认书 共 14 页
(These specifications are composed of 14 pages, including this title page.)

| 宁 波 舜 宇 光 电 信 息 有 限 公 司 | | |
|---|---|---|
| 批 准 (Approved) | 审 核 (Checked) | 担 当 (In charge) |
| | | |

# Revise History

| Rev | Date | Description |
|---|---|---|
| Ver1.0 | 2010-11-04 | Draft |
| Ver1.1 | 2010-12-03 | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

# 1. Scope

This approval sheet contains the general information of Q3S06A QXGA camera module designed for NINGBO SUNNY OPOTECH CO.,LTD. It contains the key features of the module as well as the information for the quality inspection and reliability test purposes.

# 2. General Description

The Camera Module includes: Samsung CMOS Sensor(S5K4CDGX), Lens, Holder,Connector and FPC .

The S5K4CDGX is a highly integrated Quadruple XGA (QXGA) camera chip that includes a CMOS image sensor (CIS),Image Signal Processor (ISP) and JPEG on the fly. It is fabricated by the SAMSUNG 90nm CMOS image sensor process developed for imaging applications, to realize high-efficiency and low-power photo sensor. The sensor consists of 2048 x 1536 effective pixels that meet with 1/4 inch optical format. The CIS has on-chip 10-bit ADC arrays to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. The ISP performs sophisticated image processing functions including color recovery and correction, edge enhancement, lens shading correction, programmable gamma correction, auto defect correction, auto flicker correction, auto focus (AF), auto Exposure (AE), auto white balance (AWB), and image scaling. The AF, AE and AWB functions are preformed by an embedded RISC processor. The host controller is able to access and control this device via the I2C bus.

## Features

- QXGA format sensor with 1/4″ optics
- Full resolution@15fps,VGA@30fps
- JPEG on-the-fly compression with embedded JPEG file size control
- JPEG image rotation support
- 10-bit parallel video interface,8-Bit ITU-R.656/601
- Continuous pseudo zoom
- Standard frame spoof mode for JPEG8.Status and Pointers to interleaved video lines embedded in frame footer.
- Fully integrated and programmable Image Signal Processor(ISP)
- Automatic adjustment to diverse lighting conditions
- Auto focus supports single shot or tracking focus for continuous operation
- Low-power HW and SW standby modes,as well as low power reduced resolution modes
- Xenon and Ledflash support
- Embedded PLL enables fine output data rate clock freq control,with an input clock frequency of 6MHz-56MHz
- Variable frame rate up to 15fps for QXGA and up to 30fps for VGA
- Slave Serial Control interface:I2C-compatible interface with host for programming and register read-back
- Integrated ADC to support AF
- On chip OTP memory to support Chip ID(48bit) and module to module compensation(192 bit)

## 2.1 General Description

### 2.1.1 Sensor Specification

| No. | Item | Specification |
|---|---|---|
| 1 | Sensor | S5K4CDGX |
| 2 | Optical format | 1/4 inch |
| 3 | Pixel Size | 1.75μm×1.75μm |
| 4 | Active pixels | 2048(H) x 1536(V),QXGA |
| 5 | Output format | YUV422,RGB565,RGB888,RAW8,RAW10,JPEG,Interleaved JPEG8(SOSI,EOSI,SOEI,EOEI),Interleaved JPEG/Video(by data type) |
| 6 | Supply voltage | 2.8V for analog and 2.8V or 1.8V for I/O, 1.5V for digital core supply |
| 7 | Operating temperature | -20℃ to +60℃ |

### 2.1.2 Lens Specification

| No. | Item | Specification |
|---|---|---|
| 1 | Lens Size | 1/4″ |
| 2 | Lens Construction | 4P+1IR Filter |
| 3 | Focal Length | 3.29mm |
| 4 | F/NO. | 2.8 |
| 5 | Field of View Angle (Diagonal) | 69.1° ±3° |
| 6 | Image Quality | ≥800LW/PH |
| 7 | Focusing Range | 10CM- ∞ |

### 2.1.3 Auto-Focus Specification

| No. | Item | Specification |
|---|---|---|
| 1 | VCM Type (KAF-V85S60-21) | 8.5*8.5*3.4 |
| 2 | Absolute Max Current | 100mA |
| 3 | VCM Drive | AD5820 |

## 2.2 Sensor Electrical Specification

### 2.2.1 Absolute Maximum Rating

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| I/O Power (1.65 ~ 3.0V) | VDDIO | -0.3 to 3.8 | V |
| Analog Power (2.8V) | VDDA | -0.3 to 3.8 | |
| Regulator Power (1.8V) | VDDD_REG | -0.3 to 3.8 | |
| Digital Power (1.5V) | VDDD | -0.3 to 2.0 | |
| Operating Temperature | VOPR | -20 to +60 | ℃ |
| Storage Temperature | VSTG | -40 to +85 | |

### 2.2.2 Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Vtol | Tolerant Voltage | - | - | 3.0 | V | Power off mode |
| $V_{DDA}$ | Analog Supply Voltage | 2.6 | 2.8 | 3.0 | V | |
| $V_{DDD\_REG}$ | Regulator Supply Voltage | 1.7 | 1.8 | 1.9 | V | |
| $V_{DDIO1}$ | IO power (option 1) | 2.6 | 2.8 | 3.0 | V | |
| $V_{DDIO2}$ | IO power (option 2) | 1.65 | 1.8 | 1.95 | V | |
| $V_{DDD}$ | Digital Supply Voltage (regulator output) | 1.4 | 1.5 | 1.6 | V | |
| Temp | Ambient Temperature | -20 | 25 | 60 | ℃ | |
| Vih | DC Input Logic High | 0.7*$V_{DD}$ | - | - | V | |
| Vil | DC Input Logic Low | - | - | 0.3*$V_{DD}$ | V | |
| VT | Switching Threshold | - | 0.5*$V_{DD}$ | - | V | |
| VT+ | Schimtt trigger, positive | - | - | 0.7*$V_{DD}$ | V | |
| VT- | Schimitt trigger, negative | 0.3*$V_{DD}$ | - | - | V | |

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Iih | High Level Input Current | -10 | - | 10 | uA | No pull-down option |
| Iil | Low Level Input Current | -10 | - | 10 | uA | No pull-up option |
| Voh | Output High Voltage(@Ioh=-100uA) | VDD-0.2 | - | - | V | |
| Vol | Output Low Voltage(@Iol=100uA) | - | - | 0.2 | V | |
| FIN (with PLL) | Input Operating Frequency | 6 | - | 56 | MHz | Min 12.8Mhz requiered for Fast I2C operation |
| FOUT | Output Operating Frequency | 6 | 48/96/104 | 116 | MHz | Typ – depending on application |
| COUT | External Load Capacitance | - | - | 5 | pF | |
| ISTBY[2] | HW Standby Current (VDDD 1.8V) | - | 12 | 30 | uA | |
| | HW Standby Current (VDDA 2.8V) | - | 6 | 20 | | |
| | HW Standby Current (VDDIO 2.8V) | - | 4 | 10 | | |
| P (Capture)[2] | Power Consumption (VDDD 1.8V) | - | 224 | 306 | mW | 2048x1536 @ 15 fps<br>PCLK disabled in Blank |
| | Power Consumption (VDDA 2.8V) | - | 176 | 182 | | |
| | Power Consumption (VDDIO 2.8V)[1] | - | 67 | 73 | | |
| | Total Power Consumption | - | 467 | 561 | | |
| P (Preview)[2] | Power Consumption (VDDD 1.8V) | - | 169 | 230 | mW | 640x480 @ 30 fps<br>PCLK disabled in Blank |
| | Power Consumption (VDDA 2.8V) | - | 165 | 170 | | |
| | Power Consumption (VDDIO 2.8V)[1] | - | 14 | 16 | | |
| | Total Power Consumption | - | 348 | 416 | | |

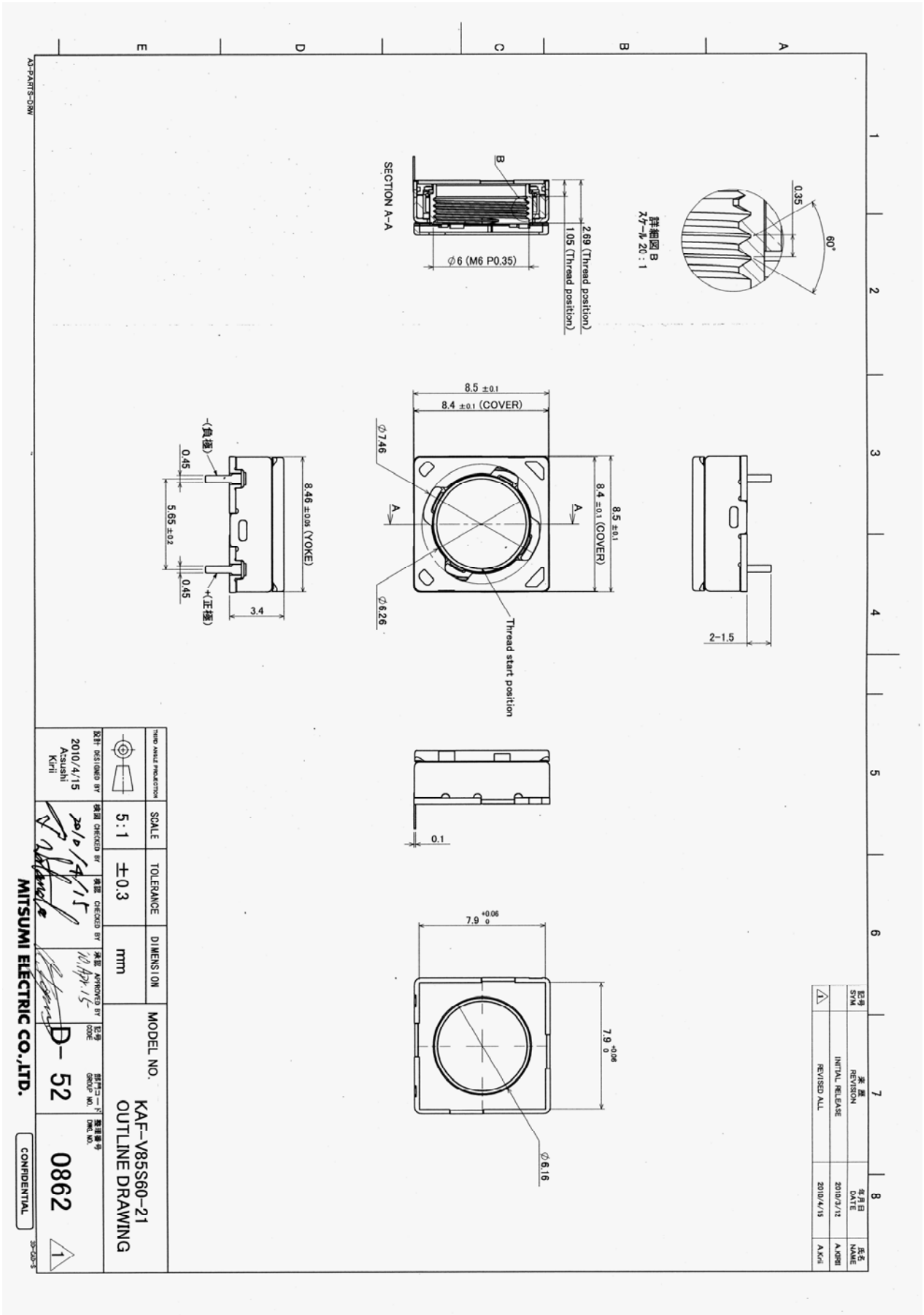
[Notes]

(1) $P_{VDDIO}$ is affected by external PCB capacitance.

(2) Max current spec is at 55°C

NOTE: For more information please refer to S5K4CDGX datasheet

# 2.3 VCM (Voice Coil Motor) Specification(KAF-V85S60-21)



## 2.4 VCM Driver AD5820 Specification

The AD5820 is a single 10-bit DAC with 100mA output current sink capability. It features an internal reference and operates from asingle 2.3 V to 5.5 V supply. The DAC is controlled via a 2-wire (I2C-compatible) serial interface that operates at clock rates up to 400 kHz.

The AD5820's unique and proprietary Slew Rate Control Modes allow the user to customize the output transient response thereby overcoming mechanical ringing associated with reduced form factor voice coil motors (VCMS).

The AD5820 also incorporates a power-on reset circuit, which ensures that the DAC output powers up to 0 V and remains there until a valid write takes place. It has a power-down feature that reduces the current consumption of the device to 1 μA maximum.

The AD5820 is designed for autofocus, image stabilization, and optical zoom applications in camera phones, digital still cameras, and camcorders.

The AD5820 also has many industrial applications, such as controlling temperature, light, and movement, over the range −40° C to +85° C without derating.

The I2C address for the AD5820 is 0x18h.

Table 4. Timing Specification (See Figure 4,5,6)

| Parameter (NOTE1) | B Version | Unit | Description |
|---|---|---|---|
| | Limit at TMIN , TMAX | | |
| fSCL | 400 | kHz max | SCL clock frequency |
| t1 | 2.5 | μs min | SCL cycle time |
| t2 | 0.6 | μs min | tHIGH, SCL high time |
| t3 | 1.3 | μs min | tLOW, SCL low time |
| t4 | 0.6 | μs min | tHD, STA, start/repeated start condition hold time |
| t5 | 100 | ns min | tSU, DAT, data setup time |
| t6 (NOTE2) | 0.9 | μs max | tHD, DAT, data hold time |
| t7 | 0 | μs min | tSU, STA, setup time for repeated start |
| t8 | 0.6 | μs min | tSU, STO, stop condition setup time |
| t9 | 0.6 | μs min | tBUF, bus free time between a stop condition and a start condition |
| t10 | 1.3 | μs min | tR, rise time of both SCL and SDA when receiving |
| t11 | 300 | ns max | May be CMOS driven |
| | 0 | ns min | tF, fall time of SDA when receiving |
| | 250 | ns max | tF, fall time of both SCL and SDA when transmitting |
| Cb | 300 | ns max | Capacitive load for each bus line |
| | 20+0.1Cb(NOTE3) | ns min | |
| | 400 | pF max | |

NOTE:

1. Guaranteed by design and characterization; not production tested.

2. A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the VIH MIN of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

3. Cb is the total capacitance of one bus line in pF. tR and tF are measured between 0.3 VDD and 0.7 VDD.

Figure 4. 2-Wire (I2C) Serial Interface Timing Diagram

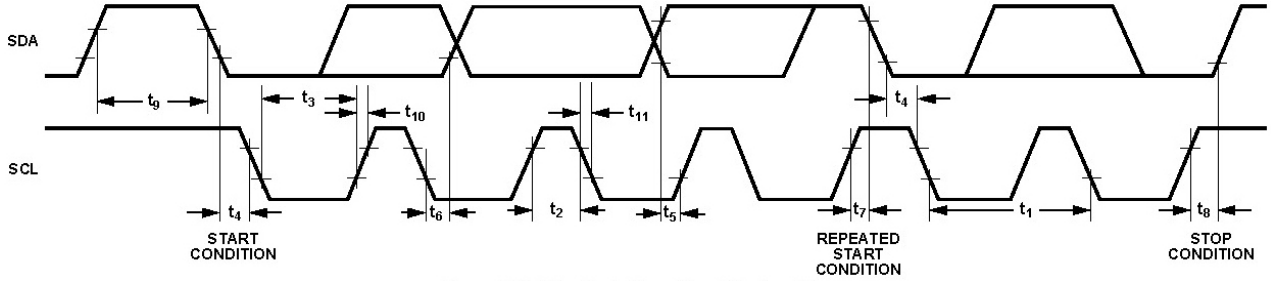



Figure 5. Write Operation

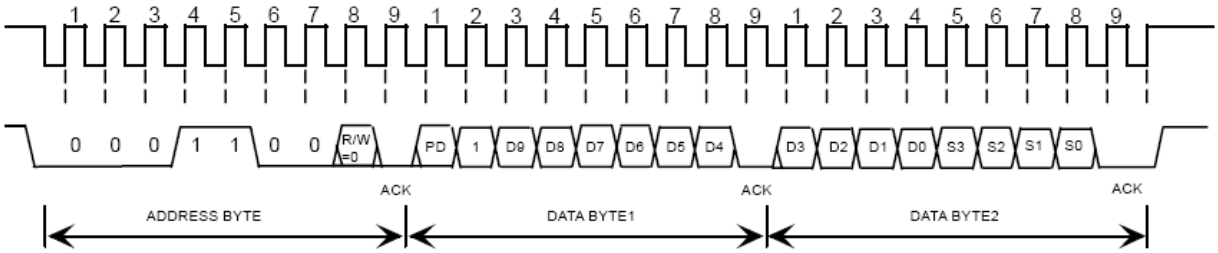



*Figure 17. Write Operation R/W = 0*

Figure 5. Read Operation

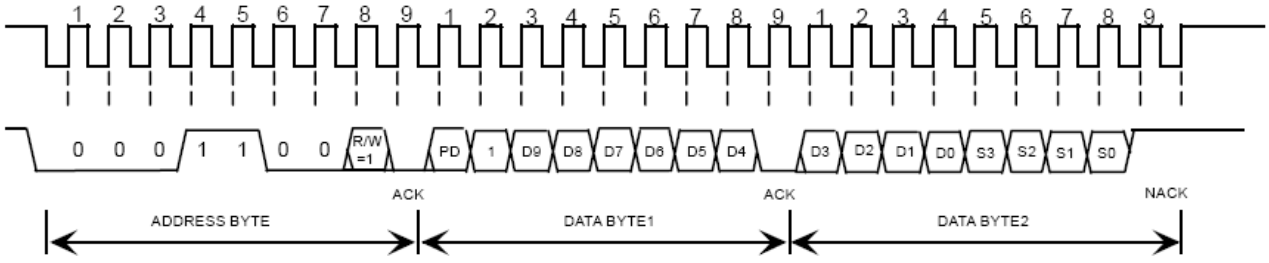


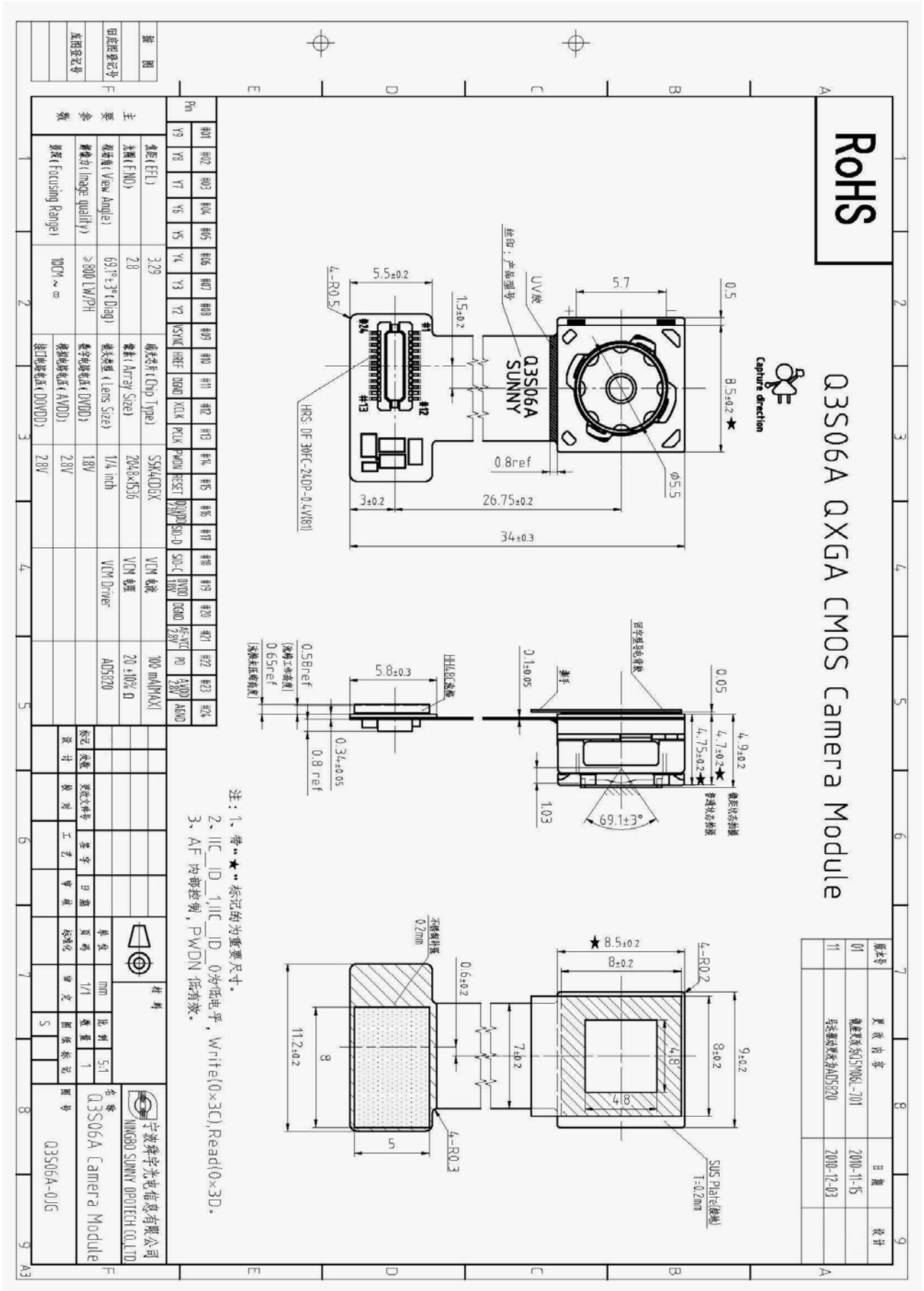

*Figure 18. Read Operation R/W = 1*

Figure 6. Data Format

| Serial Data-Words | High Byte | | | | | | | | Low Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Serial Data Bits | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |
| Input Register | R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| Function | OD | 1 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | S3 | S2 | S1 | S0 |

[1] PD = software power-down; D9 to D0 = DAC data; S3,S2,S1,S0 = Output current slew rate control.

# 3. Camera Module Configuration Specification



# 4 Camera Module PIN Description

| Pin Number | Name | Pin Type | Function/Description |
|---|---|---|---|
| Pin 1# | Y9 | Output | Data output bit[9] |
| Pin 2# | Y8 | Output | Data output bit[8] |
| Pin 3# | Y7 | Output | Data output bit[7] |
| Pin 4# | Y6 | Output | Data output bit[6] |
| Pin 5# | Y5 | Output | Data output bit[5] |
| Pin 6# | Y4 | Output | Data output bit[4] |
| Pin 7# | Y3 | Output | Data output bit[3] |
| Pin 8# | Y2 | Output | Data output bit[2] |
| Pin 9# | VSYNC | Output | Vertical sync output |
| Pin 10# | HREF | Output | HSYNC output |
| Pin 11# | DGND | Ground | Digital ground |
| Pin 12# | XCLK | Input | System clock input |
| Pin 13# | PCLK | Output | Pixel clock output |
| Pin 14# | PWDN | Function (default = 0) | Power Down Mode Selection - active high, internal pull-down resistor.<br>0: Normal mode<br>1: Power down mode |
| Pin 15# | RESET | Input | Clears all registers and resets them to their default values.<br>1: Normal mode<br>0: Reset mode |
| Pin 16# | DOVDD | Power | Digital power supply for I/O |
| Pin 17# | SIO_D | I/O | SCCB serial interface data I/O |
| Pin 18# | SIO_C | Input | SCCB serial interface clock input |
| Pin 19# | DVDD | Power | Power supply for digital logic core |
| Pin 20# | DGND | Ground | Digital ground |
| Pin 21# | AF-VCC | Power | AF Power |
| Pin 22# | PD | Power | asynchronous power down signal |
| Pin 23# | AVDD | Power | Analog power supply |
| Pin 24# | AGND | Ground | Analog ground |

## 5. Reliability Test

| No. | Test Item | Test Conditions | Judge Standard |
|---|---|---|---|
| 1 | Constant Temperate and Humidity Storage Test | Temperate: 60±3℃;<br>Humidity: 90±3%RH;<br>Test duration: 96H | No image distort and good color rendition. |
| 2 | High Temperate Storage Test | Temperate: 80±3℃;<br>Test duration: 96H | No image distort and good color rendition. |
| 3 | Low Temperate Storage Test | Temperate: -40±3℃;<br>Test duration: 96H | No image distort and good color rendition. |
| 4 | High and Low Temperate Shock Test | High Temp.: 80 ± 3℃;<br>Low Temp.: -40 ± 3℃;<br>Each Place Time: 30min;<br>Number of Cycles: 30 | No image distort and good color rendition. |
| 5 | High Temperate Function Test | Temperate: 60±3℃;<br>Test Duration: 96H;<br>Max Work Voltage | No image distort and good color rendition. |
| 6 | Low Temperate Function Test | Temperate: -20±3℃;<br>Test Duration: 96H;<br>Max Work Voltage | No image distort and good color rendition. |
| 7 | Constant Temperate and Humidity Function Test | Temperate: 55±3℃;<br>Humidity: 85%RH;<br>Test Duration: 96H;<br>Max Work Voltage | No image distort and good color rendition. |
| 8 | Vibration Test | Frequency Range: 10-50-10Hz;<br>Amplitude: 2mm;<br>Test All 3 Axes (X, Y, Z);<br>Duration 30min for Each Axis | No image distort and good color rendition. |
| 9 | ESD TEST | 8KV Contact Discharge<br>12KV Air Discharge<br>10 Times for Second | No image distort and good color rendition. |
| 10 | Package Test | Floor: Concrete;<br>Height: 100cm;<br>Positions: 1corner, 3edge, 6 Surface;<br>Each Surface Drop 3 Times | No image distort and good color rendition. |

# 6. Packaging

## 6.1. Packaging Process

1. Every module is placed into a tray until all empty slots of a tray are filled. Each tray contains no more than 45 modules.

2. Each tray use an anti-static bag to prevent the module from moisture by partially socking out the air from the stack.

3. A stack have 10 trays.

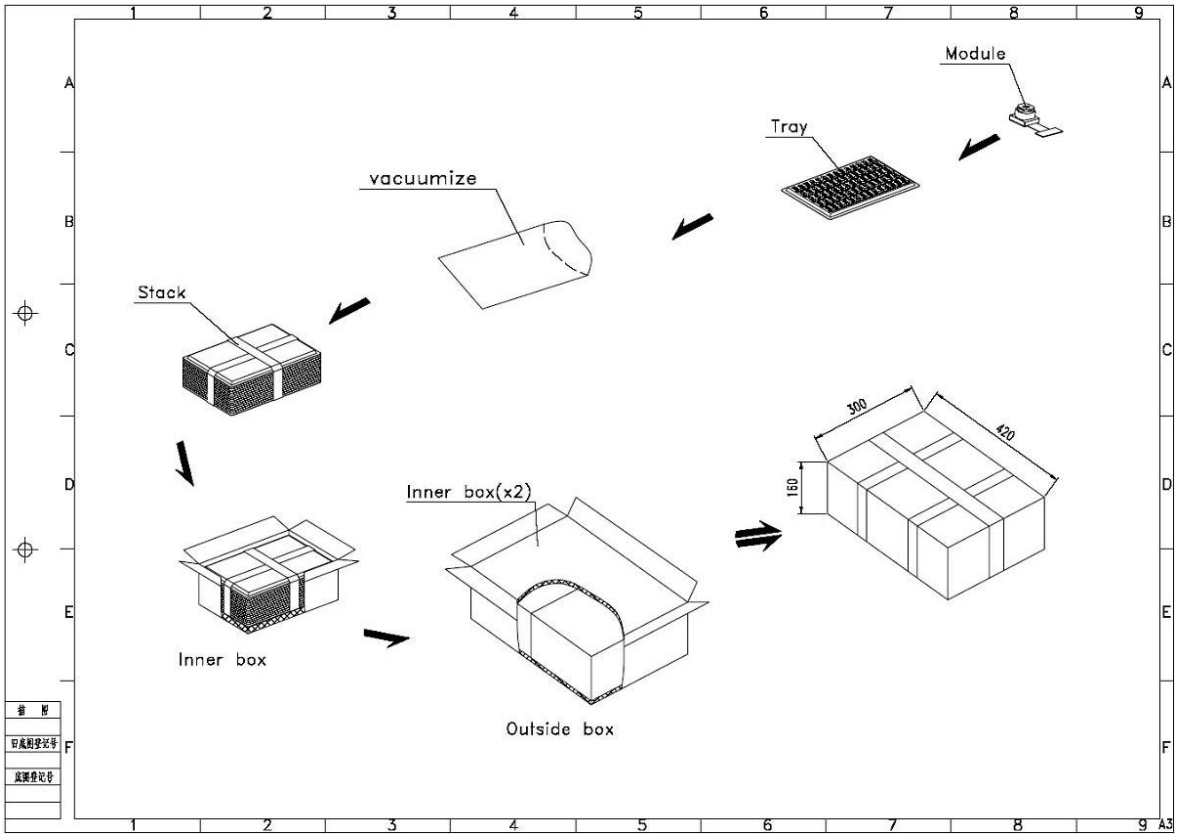
4. Insert a stack into a inner box.

5. Insert two inner boxes into a outside box. Then attach the label onto the outside box.

## 6.2. Labeling

The default label for each outside box should have the following information:
Customer:
Customer Part Number:
P.O Number:
Total Quantity:
Sunny Part Number:
Date Code:
Lot Number:
Pack Date:
Remark:

## 6.3. Sketch Map of Packing Process



# 7. Precautions

## 7.1. Storage and Operating Conditions

To keep the product and packaging material in good condition, care must be taken to control temperature and humidity in the storage area.

Recommended conditions:

Ambient temperature: 0～+40℃

Humidity: 30～70%RH

No rapid change on temperature and humidity.

The products listed in this catalog are not designed for use under the following conditions. Storage and/or usage under following conditions is prohibited.

1). Exposure to corrosive gas such as chlorine, hydrogen sulfide, ammonia, sulfur dioxide, nitrogen oxide, etc.

2). Exposure to direct sunlight.

3). Exposure to dust.

4). Exposure to excessive moisture or wet locations.

5). Exposure to salt water or sea breezes.

6). Exposure to strong static electricity or electromagnetic waves.

## 7.2. Transportation and Handling

1). Minimize any mechanical vibration or shock and avoid dropping of the product during transportation or dropping the product that contains the substrate.

2). Since the application of static electricity or over voltage may cause defect in the product or deterioration of its reliability, caution must be taken against exposure to any static electricity generated by electrified items such as workbenches, soldering irons, tools, carrying containers, etc.

3). Caution shall be taken to avoid overstress to the product.

- END -